

WHAT IS CLAIMED IS:

- 1 1. A semiconductor chip package comprising:  
2 an integrated circuit chip;  
3 a chip contact pad formed on a first side of the chip;  
4 a stud formed on the chip contact pad, the stud being formed from wire using a wire  
5 bonding machine, the stud having an elongated portion extending from the chip contact pad;  
6 a substrate comprising  
7 a first layer of insulating material on a first side of the substrate,  
8 a well formed in the first layer and opening to the first side of the substrate, the  
9 well having a bottom,  
10 a first conductive material that at least partially fills the well, and  
11 a second layer having conductive trace lines formed therein, wherein the first  
12 conductive material is electrically connected to at least one of the trace lines; and  
13 wherein the stud is partially embedded in the first conductive material to form an  
14 electrical connection between the chip and the substrate, and wherein the first side of the chip  
15 faces the first side of the substrate.
- 1 2. The semiconductor chip package of claim 1, further comprising:  
2 a conductive liner at least partially lining the well, wherein the first conductive material  
3 in the well is electrically connected to the at least one trace line via the conductive liner.
- 1 3. The semiconductor chip package of claim 1, wherein the conductive liner comprises  
2 copper.

1 4. The semiconductor chip package of claim 1, wherein the stud comprises gold and  
2 wherein the outermost surface of the contact pad comprises gold.

1 5. The semiconductor chip package of claim 1, wherein the insulating material of the first  
2 substrate layer comprises an organic material.

1 6. The semiconductor chip package of claim 1, wherein the first conductive material  
2 comprises solder.

1 7. The semiconductor chip package of claim 1, wherein the first conductive material  
2 comprises a conductive adhesive.

1 8. The semiconductor chip package of claim 1, wherein the substrate further comprises:  
2 two or more layers having conductive trace lines formed therein;  
3 a second side opposite the first side,  
4 a terminal on the second side,  
5 a via filled with a second conductive material, wherein the terminal is electrically  
6 connected to the second conductive material in the via, wherein the second conductive material  
7 is electrically connected to at least one of the conductive trace lines, and wherein the terminal is  
8 electrically connected to the chip contact pad via the stud, the first conductive material, at least  
9 one of the conductive trace lines, and the second conductive material.

1 9. The semiconductor chip package of claim 1, further comprising:  
2 a support member extending from the first layer of the substrate between the chip and the  
3 substrate, wherein the chip is at least partially supported by the support member.

1 10. The semiconductor chip package of claim 9, wherein the support member comprises  
2 polymer material.

1 11. The semiconductor chip package of claim 1, further comprising an underfill material  
2 located between the chip and the substrate.

1 12. The semiconductor chip package of claim 1, wherein the stud has a partially squashed  
2 ball portion bonded to the chip contact pad, and wherein the elongated portion extends from the  
3 partially squashed ball portion.

1 13. A method of forming a semiconductor chip package, comprising:  
2 wire bonding a wire onto a chip contact pad on a first side of an integrated circuit chip  
3 with a wire bonding machine;  
4 severing the wire so that an elongated portion of the wire remains extending from the  
5 chip contact pad to form a stud;  
6 immersing at least part of the elongated portion of the stud into a first conductive material  
7 to form an electrical connection between the chip and a substrate, wherein the first conductive  
8 material is formed in a well, wherein the well is formed in a first layer of the substrate, wherein  
9 the well opens to a first side of the substrate, wherein the well has a bottom, wherein the first  
10 conductive material is electrically connected to a trace line formed in a second layer of the  
11 substrate, wherein the first substrate layer is over the second substrate layer, and such that the  
12 first side of the chip faces the first side of the substrate.

1 14. The method of claim 13, wherein the wire has a ball-shaped tip prior to the wire bonding,  
2 and wherein the ball-shaped tip becomes partially squashed against the chip contact pad during  
3 the wire bonding.

1 15. The method of claim 13, wherein the first conductive material comprises a conductive  
2 adhesive, and wherein the method further comprises:  
3 at least partially filling the well with the first conductive material; and  
4 curing the first conductive material after the immersing.

1 16. The method of claim 13, wherein the first conductive material comprises solder, and  
2 wherein the method further comprises at least partially melting the solder before the immersing.

1 17. A semiconductor chip package comprising:  
2 an integrated circuit chip;  
3 a chip contact pad formed on a first side of the chip;  
4 a stud formed on the chip contact pad, the stud having an elongated portion extending  
5 from the ship contact pad;  
6 a substrate comprising  
7 a first layer of insulating material on a first side of the substrate,  
8 a well formed in the first layer and opening to the first side of the substrate, the  
9 well having a bottom,  
10 a conductive liner at least partially lining the well,  
11 a first conductive material that at least partially fills the well, and  
12 a second layer having conductive trace lines formed therein, wherein the first  
13 conductive material is electrically connected to at least one of the trace lines via the conductive  
14 liner; and  
15 a support member extending from the first layer of the substrate between the chip and the  
16 substrate, wherein the stud is partially embedded in the first conductive material to form an  
17 electrical connection between the chip and the substrate, wherein the first side of the chip faces  
18 the first side of the substrate, and wherein the chip is at least partially supported by the support  
19 member.

1 18. The semiconductor chip package of claim 17, wherein the stud has a partially squashed  
2 ball portion bonded to the chip contact pad, and wherein the elongated portion extends from the  
3 partially squashed ball portion.

1 19. The semiconductor chip package of claim 17, wherein the first conductive material  
2 comprises solder.

1 20. The semiconductor chip package of claim 17, wherein the first conductive material  
2 comprises a conductive adhesive.